Claim Amendments

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A network interface, comprising:

circuitry to receive and transmit network data;

a direct memory access unit;

circuitry to maintain at least one statistic metering operation of the network interface;

circuitry, operationally coupled to the direct memory access unit, to initiate direct memory access transfer of at least one of the at least one statistic metering operation of the network interface, wherein the circuitry to initiate direct memory access transfer initiates direct memory transfer in response to at least one selected from the group of: (1) at least one configured time interval, and (2) when at least one of the at least one statistic reaches a configured threshold.

2. (original) The network interface of claim 1, wherein the at least one statistic comprises at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

3. (original) The network interface of claim 2, wherein the circuitry comprises circuitry to include a timestamp with the direct memory access transfer of the at least one statistic.

4. (original) The network interface of claim 2, wherein the circuitry comprises circuitry to include a sequence count with the direct memory access transfer of the at least one statistic, the sequence count distinguishing different sets of the at least one statistic.

5. (original) The network interface of claim 1, wherein the at least one statistic comprises at least one statistic derived from multiple packets.

6. (original) The network interface of claim 1, wherein the network interface comprises circuitry, operationally coupled to the direct memory access unit, to initiate direct memory access transfer of received network data.

7. (original) The network interface of claim 1, wherein the network interface comprises a framer.

8. (original) The network interface of claim 7, wherein the network interface comprises a Media Access Controller (MAC).

9. (original) The network interface of claim 1, wherein the network interface comprises a PHY.

10. (original) The network interface of claim 1, further comprising circuitry to configure the circuitry to initiate direct memory access transfer.

11. (original) The network interface of claim 10, wherein the circuitry to configure comprises circuitry to respond to at least one of the following: a request to transfer at least one of the at least one statistics, an indication of at least one time to initiate a transfer, at least one indication of at least one statistic to transfer, an indication of the location in memory in which to transfer the at least one statistic, and a schedule of statistic transfers.

12. (original) The network interface of claim 10, wherein the circuitry to configure comprises at least one register.

13. (original) The network interface of claim 10, wherein the circuitry to configure comprises circuitry to determine configuration information from received packets.

14. (original) The network interface of claim 13, wherein the circuitry to determine configuration information from received packets comprises circuitry to intercept packets traveling along a transmit path.

15. (original) The network interface of claim 1, wherein the direct memory access unit comprises circuitry to notify a processor of completion of a transfer.

16. (currently amended) A method, comprising:

maintaining statistics, at a network interface, metering operation of the network interface; and

transferring, by direct memory access, from the network interface to a memory accessed by at least one processor at least one of the statistics metering operation of the network interface in response to at least one statistic reaching a configured threshold.

17. (original) The method of claim 16, further comprising:

transferring packets from the network interface to the memory by direct memory access.

18. (original) The method of claim 16, wherein the at least one of the statistics comprises at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

19. (currently amended) The method of claim 16, [[,]] further comprising transferring at least one of a timestamp and a sequence number with the at least one of the statistics.

20. (original) The method of claim 16, wherein the network interface groups digital bits into frames.

21. (original) The method of claim 16, further comprising configuring the transfer of the at least one of the statistics.

22. (original) The method of claim 21, wherein the configuring comprises configuring at least one of the following: at least one subset of the statistics to transfer, at least one time to initiate a transfer, and at least one memory location to receive transferred data.

23. (original) The method of claim 21,

further comprising receiving a packet at the network interface; and

wherein the configuring comprises configuring based on data included in the packet.

24. (original) The method of claim 16,

wherein the transferring into the memory comprises transferring into a cache memory of at least one of the at least one processors.

25. (original) The method of claim 16,

further comprising signaling at least one of the at least one processors when the transfer completes.

26. (currently amended) A program product, disposed on a computer readable medium, comprising instructions for causing programmable circuitry of a network interface to:

maintain statistics metering operation of the network interface; and

initiate transfer, by direct memory access, from the network interface to memory accessed by at least one processor at least one of the statistics metering operation of the network interface in response to at least one configured time interval.

27. (original) The program of claim 26, further comprising instructions for causing the programmable circuitry to:

transfer packets from the network interface to the memory by direct memory access.

28. (original) The program of claim 26, wherein the at least one of the statistics comprises at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

29. (original) The program of claim 26, further comprising instructions for causing the programmable circuitry to include in the direct memory access transfer at least one of a timestamp and a sequence number with the at least one of the statistics.

30. (original) The program of claim 26, further comprising instructions for causing the programmable circuitry to configure the transfer of the at least one of the statistics.

31. (original) The program of claim 30, wherein the instructions for causing the programmable circuitry to configure comprise instructions for causing the programmable circuitry to configure at least one of the following: at least one subset of the statistics to transfer, at least one time to initiate a transfer, and at least one memory location to receive transferred data.

32. (original) The program of claim 30, further comprising instructions for causing the
programmable circuitry to configure the transfer based on contents of a received packet.

33. (original) The program of claim 26, further comprising instructions for causing the programmable circuitry to signal at least one of the at least one processors when the transfer completes.

34. (currently amended) A system, comprising:

at least one processor;

memory operationally coupled to the at least one processor;

a network interface, comprising:

circuitry to receive and transmit data over a network connection;

a direct memory access unit operationally coupled to the memory;

circuitry to maintain statistics metering operation of the network interface;

circuitry, operationally coupled to the direct memory access unit, to initiate direct memory access transfer of multiple ones of the statistics metering operation of the network interface, the statistics comprising at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface wherein the circuitry to initiate direct memory access transfer initiates direct memory transfer in response to a schedule of times to initiate the transfer.

35. (original) The network interface of claim 34, further comprising circuitry to configure the circuitry to initiate direct memory access transfer.

36. (original) The network interface of claim 34, wherein the circuitry comprises circuitry to determine configuration information from packets received by the network interface.

37. (original) The network interface of claim 34, further comprising circuitry, operationally coupled to the direct memory access unit, to initiate transfer of packets received via the network connection.

38. (original) The network interface of claim 34, wherein the circuitry to initiate direct memory access transfer comprises circuitry to include at least one of a timestamp and a sequence number with the transfer of the multiple ones of the statistics.